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09/933,805	08/22/2001	Tatuya Ninomiya	500.33021CX5	8027

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	13

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/933,805	NINOMIYA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23,24,26,27,29-32 and 34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23,24,26,27,29-32 and 34-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. This action is responsive to communication filed on March 31, 2004. This amendment has been entered and carefully considered. Claims 28 and 33 are cancelled. Claims 21, 23-24, 26-27, 29-32 and 34-42 are again presented for examination.

2. The objection to claim 34 is withdrawn due to the Amendment filed on March 31, 2004.

3. The Double patenting rejection with respect to claims 21 and 24 is withdrawn due to the Terminal Disclaimer filed on March 31, 2004.

4. Applicant's arguments filed on March 31, 2004 have been fully considered but deemed to be moot in view of new ground rule rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 21 and 24 recite the limitation "the second format" in the forth line of the seventh paragraph. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21, 23-24, 26-27, 29-32 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi et al. (USPN: 5,337,414), hereinafter Hashemi in view of Nakayama et al. (USPN: 5,920,893) hereinafter, Nakayama.

As per claims 21, 24 and 40, Hashemi teaches the invention as claimed, including a storage system comprising:

- a plurality of host adaptors coupled to at least one host device, which from interfaces for the host device (e.g. see figure 1, elements 4a-d and 8c1 and 8c2, column 3, lines 57-60 and 66-68; column 4, lines 1, 11-15 and column 9, lines 4-9);
- a plurality of storage devices for storing therein data received from the host device (e.g. see column 9, lines 30-34);
- a plurality of disk adaptors each coupled to one of said storage devices, which form interfaces for said storage devices (e.g. see figure 1, elements 8d1 and 8d2, column 4, lines 27-43; column 9, line 62 and column 10, lines 24-30);
- a cache (a plurality of caches) for temporarily storing therein data transferred between said plurality of host adaptors and said plurality of disk adaptors (e.g. see figure 1a, elements 24c1 or 24c2 or 24d1 or 24d2);

- two buses coupled to said plurality of host adaptors, said plurality of disk adaptors, and said cache, and which operate as a pair of buses for transferring data among said plurality of host adaptors, said plurality of disk adaptors, and said cache, wherein each bus in said two buses is adapted to transfer different data (e.g. see figure 1a, elements 6a-b), and a memory for storing a status of which of said two buses is available for use due to a failure in the other of said two buses (e.g. see column 9, lines 28-41).

Hashemi teaches the storage system as described above. However, Hashemi does not teach the further limitation of a format converter to convert data from CKD format to the FBA format and storing the FBA format data in the cache memory. Nakayama, on the other hand, teaches the data storage format converter (embedded in the control processors 305, 306, 310 and 311 in Fig. 3) that converts the data in the CKD format to the FBA format suitable for the storage devices and stores in the cache memory (309 in Fig. 3) (e.g. see abstract and Fig. 3). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the storage system of Hashemi by adding the format converter as taught by Nakayama so the data stored in a first format (variable length record format adopted in a magnetic disc system of a general-purpose computer) sent from the host device can be converted into data of a second format (fixed length format which is adopted in a commercially available miniature type magnetic disc) suitable for the storage devices. By doing so, it would provide improved compatibility by allowing Hashemi's storage system (a) to serve broader range of applications, (b) to be compatible with wide

variety of storage devices with different formats (e.g. Magnetic disks, optical disks, flash memory etc.)

As for claims 23 and 26, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches that said memory can be referred to by an external processor (e.g. see column 9, line 1 et seq.).

As per claims 27 and 37, Hashemi teaches the invention as claimed, including a storage system comprising:

- a plurality of first logical units coupled to at least one host device, which from interfaces for the host device (e.g. see figure 1, elements 4a-d and 8c1 and 8c2, column 3, lines 57-60 and 66-68; column 4, lines 1, 11-15 and column 9, lines 4-9);
- a plurality of storage devices for storing therein data transferred from the host device (e.g. see column 9, lines 30-34);
- a plurality of second logical units coupled to said storage devices (e.g. see figure 1, elements 8d1 and 8d2, column 4, lines 27-43; column 9, line 62 and column 10, lines 24-30);
- at least one cache memory unit (a plurality of caches) for temporarily storing therein data transferred between said plurality of first logical units and said plurality of second logical units (e.g. see figure 1a, elements 24c1 or 24c2 or 24d1 or 24d2); and
- at least one pass, coupled to said plurality of first logical units, said plurality of second logical units, and said at least one cache memory unit, which transfers

data among said first logical units, said plurality of second logical units, and said at least one cache memory unit (e.g. see column 9, lines 28-41 and Fig. 1). However, Hashemi does not teach the further limitation of a format converter and the cache memory unit that stores the converted data sent through said at least one pass. Nakayama, on the other hand, teaches the data storage format converter (embedded in the control processors 305, 306, 310 and 311 in Fig. 3) that converts the data in the CKD format to the FBA format suitable for the storage (e.g. see abstract and Fig. 3). Nakayama also teaches the further limitation of having the cache memory (309 in Fig. 3) unit that stores the converted data of FBA format suitable for the storage devices sent through said at least one pass (e.g. see the abstract, Fig. 3 and Col. 6, lines 30-38). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the storage system of Hashemi by adding the format converter as taught by Nakayama so the data stored in a first format (variable length record format adopted in a magnetic disc system of a general-purpose computer) sent from the host device can be converted into data of a second format (fixed length format which is adopted in a commercially available miniature type magnetic disc) suitable for the storage devices. By doing so, it would provide improved compatibility by allowing Hashemi's storage system (a) to serve broader range of applications, (b) to be compatible with wide variety of storage devices with different formats (e.g. Magnetic disks, optical disks, flash memory etc.). By storing the data sent through said at least one pass into cache, it can increase the performance of the overall storage system since the cache is relatively faster than the storage devices.

Therefore, the host devices can write the converted data into faster cache (use it as the intermediate buffer) and start processing the next data instead of waiting for the slower storage devices to copy the converted data into them.

As per claim 29, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches the storage system further comprising a shared memory unit (CIM/DIM in Figs. 1A and 1B) which stores therein control information for controlling the first logical units, the plurality of second logical units and said at least one cache memory unit. (e.g. see Col. 3, lines 24-33 and Figs. 1A and 1B).

As per claim 30, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches the storage system wherein said at least one cache memory unit (buffers 24c1-2 and 2d1-2 in Fig. 1A) has a plurality of cache memories arranged in a duplexed form, and the shared memory unit (CIM/DIM) has a plurality of shared memories arranged in a duplexed form (e.g. see Fig. 1A).

As per claims 31-32 and 38-39, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches the storage system wherein said at least one pass (Futurebuses 6a and 6b in Fig. 1A) is a duplexed common bus, which includes:

- a control information bus coupled to the first logical units and the second logical units, which transfers control information, and
- a data transfer bus coupled to the first logical units, the second logical units and cache memory unit, which transfers data among the first logical

units, the second logical units and cache memory unit (e.g. see Fig. 1A and Col. 3, lines 50-65).

6. Claims 34-35, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi in view Nakayama, further in view of Cheney et al. (USPN: 5,285,456), hereinafter, Cheney.

As per claims 34 and 41, the combination of Hashemi and Nakayama disclose the claimed invention as described above wherein the format converter converts data of CKD into data of FBA format. However, Hashemi and Nakayama fail to teach that the format converter adds a longitudinal redundancy check (LRC) code to the data of the FBA format. Cheney, on the other hand, teaches that by adding the LRC code to the data, integrity of the control information can be verified (e.g. see Col. 4, lines 9-14). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the storage system of Hashemi by adding the CRC code to the data as taught by Cheney. In doing so, it would allow the integrity of the information data and the control information to be verified when they are transferred within the system; therefore, enhancing the system's reliability.

As per claims 35 and 42, the combination of Hashemi and Nakayama disclose the claimed invention as described above. However, Hashemi and Nakayama fail to teach that the first logical units receive the physical address information in the CKD format with the cyclic redundancy check (CRC) code on a storage space of the storage device. Cheney, on the other hand, teaches that by adding the CRC code to the data, the errors generated during transmitting the data from the host devices to the storage

devices can be detected (e.g. see Col. 2, lines 40-62). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the storage system of Hashemi by adding the CRC code to the data as taught by Cheney. In doing so, it would allow the integrity of the information data and the control information to be verified when they are transferred within the system; therefore, enhancing the system's reliability.

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi in view Nakayama, further in view of Dixon et al. (USPN: 4,637,024), hereinafter, Dixon.

As per claim 36, the combination of Hashemi and Nakayama disclose the claimed invention as described above. However, Hashemi and Nakayama, fail to teach that the format converter adds the ECC and CRC code to the data before writing it to the storage device. Dixon, on the other hand, teaches that by using the CRC code, the data can be checked/verified for any errors and if any error found in the data, using the ECC, that error can be fixed (e.g. see Col. 3, lines 24-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to employ the step of adding the ECC and CRC code to the data before storing it to the storage device as taught by Dixon in the system taught by Hashemi and Nakayama. In doing so, the data get checked and corrected before it get stored in the storage device.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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